CLAIMS

What is claimed is:

1. A lookup table (LUT) circuit, comprising:

a first LUT input terminal;

a LUT output terminal;

a multiplexer circuit having a plurality of data input terminals, a first select input terminal coupled to the first LUT input terminal, a second select input terminal, and an output terminal coupled to the LUT output terminal;

a first memory cell; and

a first logic gate having a first input terminal coupled to the first LUT input terminal, a second input terminal coupled to the first memory cell, and an output terminal coupled to the second select input terminal of the multiplexer circuit.

2. The lookup table circuit of Claim 1, wherein the first logic gate is a logical NAND gate.

3. The lookup table circuit of Claim 1, further comprising a second logic gate coupled between the first LUT input terminal and the first select input terminal of the multiplexer circuit, and further coupled between the first LUT input terminal and the first input terminal of the first logic gate, the second logic gate having an additional input terminal coupled to the first memory cell.

4. The lookup table circuit of Claim 3, wherein the first and second logic gates comprise logical NAND gates.

5. The lookup table circuit of Claim 1, wherein the lookup table circuit comprises a portion of a field programmable gate array (FPGA), and the first memory cell comprises a configuration memory cell of the FPGA.

6. The lookup table circuit of Claim 1, further comprising a plurality of memory cells coupled to the data input terminals of the multiplexer circuit.

7. The lookup table circuit of Claim 6, wherein the lookup table circuit comprises a portion of a field programmable gate array (FPGA), and the first memory cell and the plurality of memory cells all comprise configuration memory cells of the FPGA.

8. The lookup table circuit of Claim 1, wherein the multiplexer circuit comprises a plurality of N-channel transistors, each of the N-channel transistors having a first data terminal coupled to a corresponding data input terminal of the multiplexer circuit, a second data terminal coupled to the output terminal of the multiplexer circuit, and a gate terminal coupled to a corresponding select input terminal of the multiplexer circuit.

9. The lookup table circuit of Claim 8, wherein:

the multiplexer circuit further comprises a third select input terminal;

the lookup table circuit further comprises an inverting logic gate coupled between the first LUT input terminal and the third select input terminal of the multiplexer circuit; and

the multiplexer circuit further comprises a plurality of P-channel transistors, each of the P-channel transistors having a first data terminal coupled to a corresponding data input terminal of the multiplexer circuit, a second data terminal coupled to the output terminal of the multiplexer circuit, and a gate terminal coupled to one of the first and third select terminals of the multiplexer circuit.

10. The lookup table circuit of Claim 8, further comprising:

a second logic gate coupled between the first LUT input terminal and the first select input terminal of the multiplexer circuit, and further coupled between the first LUT input terminal and the first input terminal of the first logic gate, the second logic gate having an additional input terminal coupled to the first memory cell; and

an inverting logic gate having an input terminal coupled to the output terminal of the second logic gate and an output terminal coupled to a third select input terminal of the multiplexer circuit, and wherein:

the multiplexer circuit further comprises a plurality of P-channel transistors, each of the P-channel transistors having a first data terminal coupled to a corresponding data input terminal of the multiplexer circuit, a second data terminal coupled to the output terminal of the multiplexer circuit, and a gate terminal coupled to one of the first and third select terminals of the multiplexer circuit.

11. The lookup table circuit of Claim 1, wherein the multiplexer circuit further comprises third and fourth select input terminals, the lookup table circuit further comprising:

a second LUT input terminal coupled to the third select input terminal of the multiplexer circuit; and

an inverting logic gate coupled between the third and fourth select input terminals of the multiplexer circuit.

12. The lookup table circuit of Claim 1, further comprising an output buffer coupled between the output terminal of the multiplexer circuit and the LUT output terminal.

13. The lookup table circuit of Claim 12, wherein the output buffer comprises a pullup coupled to the output terminal of the multiplexer circuit.

14. A programmable lookup table (LUT) circuit, comprising:

a multiplexer circuit comprising a plurality of data input terminals, a plurality of select terminals, and an output terminal, the multiplexer circuit further comprising a programmable path therethrough from each input terminal to the output terminal, each programmable path traversing at least one logic element coupled to one of the select terminals; and

programmable means, coupled to the select terminals of the multiplexer circuit, for enabling exactly one of the programmable paths in response to a first programmed value and enabling a plurality of the programmable paths in response to a second programmed value.

15. The programmable LUT circuit of Claim 14, wherein each logic element comprises an N-channel transistor having a gate terminal coupled to one of the select terminals.

16. The programmable LUT circuit of Claim 14, wherein each logic element comprises a P-channel transistor and an associated N-channel transistor coupled in parallel, the P-channel transistor and the N-channel transistor each having a gate terminal coupled to one of the select terminals.

17. The programmable LUT circuit of Claim 14, further comprising a plurality of memory cells coupled to the data input terminals of the multiplexer circuit.

18. The programmable LUT circuit of Claim 17, wherein the programmable LUT circuit comprises a portion of a field programmable gate array (FPGA), and the plurality of memory cells comprise configuration memory cells of the FPGA.

19. The programmable LUT circuit of Claim 14, further comprising an output buffer having an input terminal coupled to the output terminal of the multiplexer circuit.

20. The programmable LUT circuit of Claim 19, wherein the output buffer comprises a pullup coupled to the output terminal of the multiplexer circuit.

21. The programmable LUT circuit of Claim 14, wherein the first programmed value is a high value and the second programmed value is a low value.

22. The programmable LUT circuit of Claim 14, wherein the programmable means comprises:

a first LUT input terminal;

a first memory cell; and

a first logic gate having a first input terminal coupled to the first LUT input terminal, a second input terminal coupled to the first memory cell, and an output terminal coupled to a first select input terminal of the multiplexer circuit.

23. The programmable LUT circuit of Claim 22, wherein the first logic gate is a logical NAND gate.

24. The programmable LUT circuit of Claim 22, further comprising a second logic gate coupled between the first LUT input terminal and a second select input terminal of the multiplexer circuit, and further coupled between the first LUT input terminal and the first logic gate, the second logic gate having an additional input terminal coupled to the first memory cell.

25. The programmable LUT circuit of Claim 24, wherein the first and second logic gates comprise logical NAND gates.

26. The programmable LUT circuit of Claim 22, wherein the programmable LUT circuit comprises a portion of a field programmable gate array (FPGA), and the first memory cell comprises a configuration memory cell of the FPGA.

27. The programmable LUT circuit of Claim 22, wherein the programmable means further comprises:

a second LUT input terminal;

a second memory cell; and

a second logic gate having a first input terminal coupled to the second LUT input terminal, a second input terminal coupled to the second memory cell, and an output terminal coupled to a second select input terminal of the multiplexer circuit.

28. A method of providing a logical value, the method comprising:

providing, when a first memory cell stores a first programmed value, a first stored value via a first signal path; and

providing, when the first memory cell stores a second programmed value, both the first stored value via the first signal path and a second stored value via a second signal path,

wherein both the first stored value and the second stored value have the logical value,

wherein the first and second signal paths differ from each other in at least a portion of the signal paths, and

wherein the first and second programmed values differ from each other.

29. The method of Claim 28, wherein the first memory cell comprises a configuration memory cell in a programmable logic device (PLD).

30. The method of Claim 29, further comprising:

configuring the PLD to store one of the first and second programmed values in the first memory cell.

31. The method of Claim 29, wherein the PLD is a field programmable gate array (FPGA).

32. The method of Claim 28, further comprising:

storing one of the first and second programmed values in the first memory cell.

33. The method of Claim 28, further comprising:

storing the first and second stored values in second and third memory cells.

34. The method of Claim 33, wherein the second and third memory cells comprise configuration memory cells in a programmable logic device (PLD).

35. The method of Claim 34, further comprising:

configuring the PLD to store the first and second stored values in the second and third memory cells, respectively.

36. The method of Claim 34, wherein the PLD is a field programmable gate array (FPGA).

37. The method of Claim 28, wherein the first programmed value is a high value, and the second programmed value is a low value.

38. A method of providing a logical value in a programmable logic device (PLD), the logical value being addressed by first and second signal lines, the method comprising:

utilizing a signal on the second signal line to select two of four signals comprising four stored values;

selecting, when a first memory cell stores a first programmed value, exactly one of the two selected signals based on a value on the first signal line, the exactly one signal having the logical value; and

selecting, when the first memory cell stores a second programmed value different from the first programmed value, both of the two selected signals irregardless of the value on the first signal line, the two selected signals both having the logical value.

39. The method of Claim 38, wherein the second signal line comprises a used signal line in the PLD, and the first signal line comprises an unused signal line in the PLD.

40. The method of Claim 38, wherein the first memory cell comprises a configuration memory cell of the PLD.

41. The method of Claim 40, further comprising:

configuring the PLD to store one of the first and second programmed values in the first memory cell.

42. The method of Claim 38, wherein the PLD is a field programmable gate array (FPGA).

43. The method of Claim 38, further comprising:

storing one of the first and second programmed values in the first memory cell.

44. The method of Claim 38, wherein the four stored values are stored in four additional memory cells.

45. The method of Claim 44, further comprising:

storing the four stored values in the four additional memory cells.

46. The method of Claim 44, wherein the four additional memory cells comprise configuration memory cells in the PLD.

47. The method of Claim 46, further comprising:

configuring the PLD to store the four stored values in the four additional memory cells.

48. The method of Claim 38, wherein the four stored values are provided by four multiplexer circuits.

49. The method of Claim 38, wherein at least one of the four stored values is provided by a multiplexer circuit.

50. The method of Claim 38, wherein the first programmed value is a high value, and the second programmed value is a low value.

51. A programmable lookup table (LUT) circuit, comprising:

a memory cell;

means for providing, when the memory cell stores a first programmed value, a first stored value via a first signal path; and

means for providing, when the memory cell stores a second programmed value, both the first stored value via the first signal path and a second stored value via a second signal path,

wherein the first stored value and the second stored value comprise the same logical value,

wherein the first and second signal paths differ from each other in at least a portion of the signal paths, and

wherein the first and second programmed values differ from each other.

52. A programmable lookup table (LUT) circuit providing a logical value addressed by first and second signal lines, the LUT circuit comprising:

a memory cell;

means for utilizing a signal on the second signal line to select two of four signals comprising four stored values;

means for selecting, when the memory cell stores a first programmed value, exactly one of the two selected signals based on a value on the first signal line, the exactly one signal having the logical value; and

means for selecting, when the memory cell stores a second programmed value, both of the two selected signals irregardless of the value on the first signal line, the two selected signals both having the logical value.

53. A method of providing a logical value from a lookup table (LUT) utilized in a PLD design, the LUT comprising a plurality of stored values and being controlled by a plurality of signal lines, the method comprising:

providing, when all of the signal lines controlling the LUT are used in the PLD design, exactly one of the stored values; and

increasing, when at least one of the signal lines controlling the LUT is unused in the PLD design, the speed of the LUT by providing more than one of the stored values,

wherein all of the provided more than one stored values have identical logical values.

54. The method of Claim 53, wherein:

the plurality of stored values comprises four values;

the plurality of signal lines comprises two signal lines; and

the provided more than one of the stored values comprises two stored values.

55. The method of Claim 53, wherein:

the plurality of stored values comprises sixteen values;

the plurality of signal lines comprises four signal lines; and

the provided more than one of the stored values comprises one of two, four, and eight stored values.

56. The method of Claim 55, wherein:

exactly one of the four signal lines is unused; and

the provided more than one of the stored values comprises two stored values.

57. The method of Claim 55, wherein:

exactly two of the four signal lines are unused; and

the provided more than one of the stored values comprises four stored values.

58. The method of Claim 55, wherein:

exactly three of the four signal lines are unused; and

the provided more than one of the stored values comprises eight stored values.

59. The method of Claim 53, further comprising:

configuring a PLD with the PLD design, including programming a configuration memory cell of the PLD with a first programmed value indicating that a first one of the signal lines in the PLD design is used.

60. The method of Claim 53, further comprising:

configuring a PLD with the PLD design, including programming a configuration memory cell of the PLD with a second programmed value indicating that a second one of the signal lines in the PLD design is unused.

61. The method of Claim 53, wherein the PLD design is a field programmable gate array (FPGA) design.